

STN LCD DRIVER USING CIRCUIT WITH FEWER CAPACITORS AND METHOD THEREFOR

BACKGROUND OF THE INVENTION

5 This application claims the priority of Korean Patent Application No. 2002-60672 filed on October 4, 2002, in the Korean Intellectual Property Office, the contents of which are incorporated herein in their entirety by reference.

1. Field of the Invention

10 The present invention relates to the field of Super Twisted Nematic (STN) Liquid Crystal Display (LCD) technology, and more particularly, to an STN LCD driver using a circuit with fewer capacitors for driving voltage stabilization and improving display quality by stabilizing levels of driving voltages, and a method therefor.

2. Description of the Related Art

15 In a six-level driving method of an STN LCD driver, six driving voltages are used for driving a liquid crystal display. In detail, five driving voltages and a ground voltage are used. If the driving voltages have unstable levels, display quality may be degraded. Thus, to stabilize the levels of the driving voltages, the STN LCD driver uses capacitors, each of which is connected to a respective terminal where a voltage level is generated.

20 FIG. 1 is a schematic block diagram of a conventional STN LCD driver operated according to a six-level driving method. Referring to FIG. 1, the conventional STN LCD driver includes a driving voltage generating circuit 11 for generating five driving voltages, i.e., first through fifth driving voltages V0-V4, as well as a common/segment driving circuit 13 for generating a common driving signal COM and a segment driving signal
25 SEG.

The driving voltage generating circuit 11 includes a voltage converter 111, a voltage regulator 112, and a voltage divider 113. The common/segment driving circuit 13 includes a common driver 131 and a segment driver 132.

30 In the conventional STN LCD driver, capacitors C0-C4 are connected to terminals from which driving voltages V0-V4 are generated, to stabilize the levels of driving voltages V0-V4.

However, as the capacitors C0-C4 for driving voltage stabilization occupy an increasingly large area, the entire chip area of the STN LCD driver increases. In addition, the capacitors C0-C4 for driving voltage stabilization fail to sufficiently stabilize levels of driving voltages for liquid crystal displays, thus degrading the display quality.

5

SUMMARY OF THE INVENTION

The present invention provides an STN LCD driver with a control circuit which has fewer capacitors for driving voltage stabilization and improves display quality by stabilizing levels of driving voltages.

10

The present invention also provides a method for reducing the number of capacitors for driving voltage stabilization used in an STN LCD driver and improving the display quality by stabilizing levels of driving voltages.

15

In accordance with an aspect of the present invention, there is provided an STN LCD driver comprising a driving voltage generating circuit, a common/segment driving circuit, first through third capacitors, and a control circuit. The driving voltage generating circuit generates first through fifth driving voltages and outputs the generated voltages via first through fifth output terminals. The common/segment driving circuit, controlled by a driving polarity signal, receives the first through fifth driving voltages and generates a common driving signal and a segment driving signal. The first capacitor is coupled between the first output terminal and a ground voltage. The control circuit controls connection of the output terminals and capacitors in response to the driving polarity signal.

20

25

30

It is preferred in the present invention that the control circuit include first through fourth switches. The first switch connects one end of the second capacitor to one of the first output terminal and fifth output terminal in response to the driving polarity signal. The second switch connects the other end of the second capacitor to one of the second output terminal and the ground voltage in response to the driving polarity signal. The third switch connects one end of the third capacitor to one of the second output terminal and the fourth output terminal in response to the driving polarity signal. The fourth switch connects the other end of the third capacitor to one of the third output terminal and fifth output terminal in response to the driving polarity signal.

In one embodiment, the common/segment driving circuit generates the common driving signal and the segment driving signal using the first driving voltage, fourth driving voltage, fifth driving voltage, and ground voltage, when the driving polarity signal is in a first logic state. The common/segment driving signal generates the common driving
5 signal and the segment driving signal using the first driving voltage, second driving voltage, third driving voltage, and ground voltage, when the driving polarity signal is in a second logic state.

When the driving polarity signal is in the first logic state, one end of the second capacitor is coupled to the fifth output terminal by the first switch, the other end of the
10 second capacitor is coupled to the ground voltage by the second switch, one end of the third capacitor is coupled to the fourth output terminal by the third switch, and the other end of the third capacitor is coupled to the fifth output terminal by the fourth switch.

When the driving polarity signal is in the second logic state, one end of the second capacitor is coupled to the first output terminal by the first switch, the other end
15 of the second capacitor is coupled to the second output terminal by the second switch, one end of the third capacitor is coupled to the second output terminal by the third switch, and the other end of the third capacitor is coupled to the third output terminal by the fourth switch.

In accordance with another aspect of the present invention, there is provided a
20 method for reducing the number of capacitors for driving voltage stabilization used in an LCD driver. The LCD driver includes a driving voltage generating circuit for generating first through fifth driving voltages and outputting the generated driving voltages via first through fifth output terminals, and a common/segment driving circuit, controlled by a driving polarity circuit, for receiving the first through fifth driving voltages to generate a
25 common driving signal and a segment driving signal. The method comprises connecting a first capacitor between the first output terminal and a ground voltage. When the driving polarity signal is in a first logic state, one end of the second capacitor is coupled to the fifth output terminal by the first switch, the other end of the second capacitor is coupled to the ground voltage by the second switch, one end of the third capacitor is
30 coupled to the fourth output terminal by the third switch, and the other end of the third capacitor is coupled to the fifth output terminal by the fourth switch. When the driving

polarity signal is in a second logic state, one end of the second capacitor is coupled to the first output terminal by the first switch, the other end of the second capacitor is coupled to the second output terminal by the second switch, one end of the third capacitor is coupled to the second output terminal by the third switch, and the other end of the third capacitor is coupled to the third output terminal by the fourth switch.

The common/segment driving circuit generates a common driving signal and a segment driving signal using the first driving voltage, second driving voltage, third driving voltage, and ground voltage when the driving polarity signal is in the first logic state, and generates the common driving signal and the segment driving signal using the first driving voltage, fourth driving voltage, fifth driving voltage, and ground voltage when the driving polarity signal is in the second logic state.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the invention will be apparent from the more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

FIG. 1 is a schematic block diagram of a conventional STN LCD driver operated according to a six-level driving method.

FIG. 2 is a schematic block diagram of an STN LCD driver according to an embodiment of the present invention, operated according to a six-level driving method.

FIG. 3 illustrates a voltage waveform of a common driving signal COM based on a driving polarity signal CON of the STN LCD driver shown in FIG. 2, according to a six-level driving method.

FIG. 4 illustrates a voltage waveform of a segment driving signal SEG based on a driving polarity signal COM of the STN LCD driver shown in FIG. 2, according to a six-level driving method.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 is a schematic block diagram of an STN LCD driver according to an embodiment of the present invention, operated according to a six-level driving method.

Referring to FIG. 2, the STN LCD driver of the present invention includes a driving voltage generating circuit 21 for generating first through fifth driving voltages V0-V4, and a common/segment driving circuit 23, controlled by a driving polarity signal CON, for receiving the first through fifth driving voltages V0-V4 to generate a common driving signal COM and a segment driving signal SEG.

In particular, the STN LCD driver includes a control circuit 25, with a reduced number of capacitors C5-C7 for stabilizing levels of the driving voltages V0-V4. The first capacitor C5 is connected between the output terminal from which the first driving voltage V0 is output and a ground voltage VSS, and the control circuit controls connection of the second capacitor C6 and the third capacitor C7 with the output terminals.

The voltage difference between every two adjacent driving voltages among the first through fifth driving voltages V0-V4 is the same. The common/segment driving circuit 23 includes a common driver 231 and a segment driver 232. The common driver 231, which is controlled by the driving polarity signal CON, receives the first driving voltage V0, the second driving voltage V1, the fifth driving voltage V4, and the ground voltage VSS and generates the common driving signal COM. The segment driver 232, which also is controlled by the driving polarity signal CON, receives the first driving voltage V0, the third driving voltage V2, the fourth driving voltage V3, and the ground voltage VSS and generates the segment driving voltage SEG.

The control circuit 25 includes first through fourth switches 251-254. The first switch 251 connects one end of the second capacitor C6 to the output terminal from which the first driving voltage V0 is output or the output terminal from which the fifth driving voltage V4 is output. The second switch 252 connects the other end of the second capacitor C6 to the output terminal from which the second driving voltage V1 is output or the ground voltage VSS in response to the driving polarity signal CON.

The third switch 253 connects one end of the third capacitor C7 to the output terminal from which the second driving voltage V1 is output or the output terminal from which the fourth driving voltage V3 is output in response to the driving polarity signal

CON. The fourth switch 254 connects the other end of the third capacitor C7 to the output terminal from which the third driving voltage V2 is output or the output terminal from which the fifth driving voltage V4 is output.

FIG. 3 illustrates a voltage waveform of the common driving signal COM based on the driving polarity signal CON of the STN LCD driver according to the six-level driving method, and FIG. 4 illustrates a voltage waveform of the segment driving signal SEG based on the driving polarity signal CON of the STN LCD driver according to the six-level driving method.

Hereinafter, a method for reducing the number of capacitors for driving voltage stabilization in the STN LCD driver according to the present invention of FIG. 2 will be described in detail with reference to FIGS. 3 and 4. As illustrated in FIG. 3, when the driving polarity signal CON is in a first logic state, i.e., in a logic low state, the common driving signal COM has the first driving voltage level V0 and the fifth driving voltage level V4. When the driving polarity signal CON is in a second logic state, i.e., in a logic high state, the common driving signal COM has the second driving voltage level V1 and the ground voltage level VSS.

As illustrated in FIG. 4, when the driving polarity signal CON is in a logic low state, the segment driving signal SEG has the fourth driving voltage level V3 and the ground voltage level VSS. When the driving polarity signal CON is in a logic high state, the segment driving signal SEG has the first driving voltage level V0 and the third driving voltage level V2.

Thus, when the driving polarity signal CON is in the logic low state, the common driving signal COM and the segment driving signal SEG are generated using the first driving voltage V0, fourth driving voltage V3, fifth driving voltage V4, and ground voltage VSS. When the driving polarity signal CON is in the logic high state, the common driving signal COM and the segment driving signal SEG are generated using the first driving voltage V0, second driving voltage V1, third driving voltage V2, and ground voltage VSS.

Accordingly, in the present invention, the control circuit 25 can change connection of the capacitors C5-C7 for driving voltage stabilization according to the

logic state of the driving polarity signal CON, thereby reducing the number of capacitors required for driving voltage stabilization.

For example, when the driving polarity signal CON is in the first logic state, i.e., in the logic low state, one end of the second capacitor C6 is coupled to the fifth driving voltage V4 by the first switch 251, the other end of the second capacitor C6 is coupled to the ground voltage VSS by the second switch 252, one end of the third capacitor C7 is coupled to the fourth driving voltage V3 by the third switch 253, and the other end of the third capacitor C7 is coupled to the fifth driving voltage V4 by the fourth switch 254.

Thus, when the driving polarity signal CON is in the logic low state, the third capacitor C7 and the second capacitor C6 are connected in series between the fourth driving voltage V3 and the ground voltage VSS, and the second capacitor C6 is connected between the fifth driving voltage V4 and the ground voltage VSS. Also, the third capacitor C7 is connected between the fourth driving voltage V3 and the fifth driving voltage V4. That is, when the driving polarity signal CON is in the logic low state, the capacitors for driving voltage stabilization are connected not to the driving voltages V1 and V2, but to the driving voltages V0, V3, and V4.

According to the foregoing method, unlike the conventional circuit using five capacitors for driving voltage stabilization, only three capacitors are used for driving voltage stabilization. Thus, the chip area occupied by the STN LCD driver can be decreased.

Furthermore, when an STN LCD driver is driven by the six-level driving method, the main factor affecting the display quality is a stabilization level of a relative voltage between two adjacent driving voltages V0-V1, V1-V2, V3-V4, or V4-VSS, rather than the stabilization level of each of the driving voltages V0, V1, V2, V3, and V4 individually. In the present invention, as described above, when the driving polarity signal CON is in the logic low state, i.e., when the driving voltages V0, V3, and V4 are used, the third capacitor C7 is connected between the fourth and fifth driving voltages V3 and V4 adjacent to each other. When the driving polarity signal CON is in the logic high state, i.e., when the driving voltages V0, V1, and V2 are used, the second capacitor C6 is connected between the first and second driving voltages V0 and V1 adjacent to each

other, and the third capacitor C7 is connected between the second driving voltage V1 and the third driving voltage V2 adjacent to each other.

In the present invention, a capacitor is connected between two adjacent driving voltages, thereby stabilizing the relative voltage between the two driving voltages.

5 Thus, the STN LCD driver of the present invention improves the display quality.

As set forth above, in the STN LCD driver of the present invention, the reduced number of capacitors for driving voltage stabilization enables the chip area to be scaled down. Also, since a capacitor is connected between two adjacent driving voltages, a relative voltage between the two driving voltages is stabilized, enhancing display quality.

10 While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims.

15